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Adding Binary Numbers

Full Adders

The story of adding binary numbers is still incomplete. The case arises when more than one binary digit is to be added to a similar sized binary number such as the following.

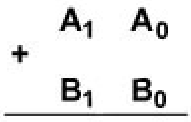


Figure 1 Adding Two - Two Digit Binary Numbers

There are two binary numbers to be added. They are; A_1 A_0 and B_1 B_0

Applying the rules for adding single digits, we can proceed to add the "right most digits"- (LSB's) first. However that adding these digits; $\mathbf{A_0}$ to $\mathbf{B_0}$ yields a "sum" $\mathbf{S_0}$ and a "carry" $\mathbf{C_0}$

But now we are stuck with somewhat of a problem. The carry C_0 now needs to be added to the two digits in the "next highest place" as shown here.

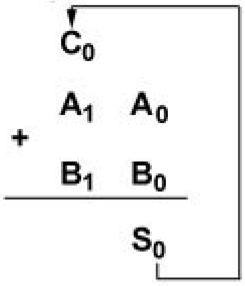


Figure 2 Sum and Carry Results of Adding the First-Place(LSB) Digits of a Two Digit Binary Numbers

As can be seen in figure 12, there are now **three digits to be added together $\mathbf{C_0}$, $\mathbf{A_1}$ and $\mathbf{B_1}$**, not two as we have been shown how to do previously.

Now it is possible to built a "new" circuit that will add three digits which we will call a "full adder". Since we have no idea as to the values of each of these three digit, we must account for every combination. As in the case of the half adder, a truth-table must be constructed demonstrating all of the possible algebraic addition combinations for three digits.

Something worth noting is that the sum of three digits will also yield a "new" sum S_1 and a "new" carry C_1 as shown in figure 13 below.

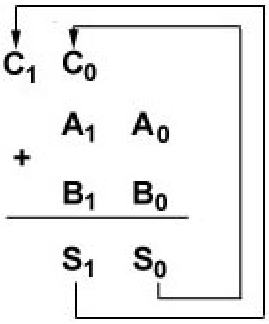


Figure 3 Sum and Carry Results of Adding Two - Two Digit Binary Numbers

It goes without saying that this diagrammatic scheme can be extended to any number of bits to be added. This will become important to consider as we proceed with the topic of adding BCD digits.

A truth table can be constructed for adding 3 bits and is given in figure 14 below.

Bits to Be Added			**New Sum & Carry-Out**	
C_{n-1}	A_n	B_n	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 4 Truth-Table for Adding 3-Bits Showing the Resultant Sum and Carry

By using the same technique, we can easily observe that this logic system has three inputs and two outputs.

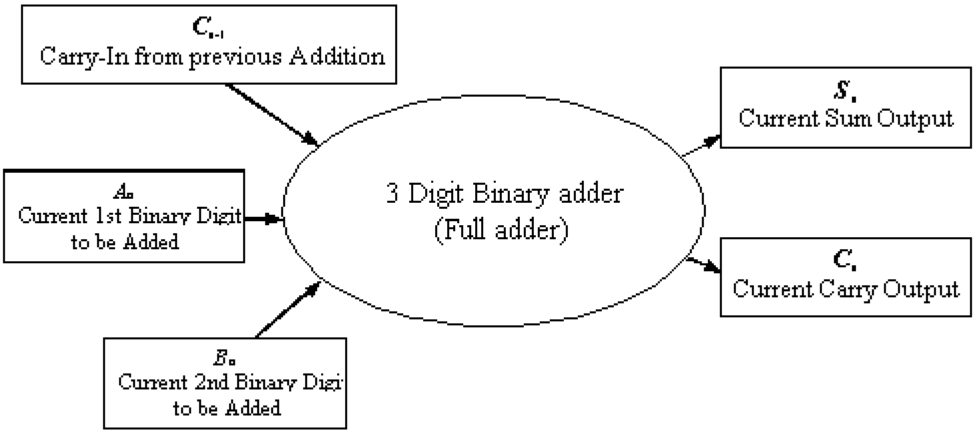


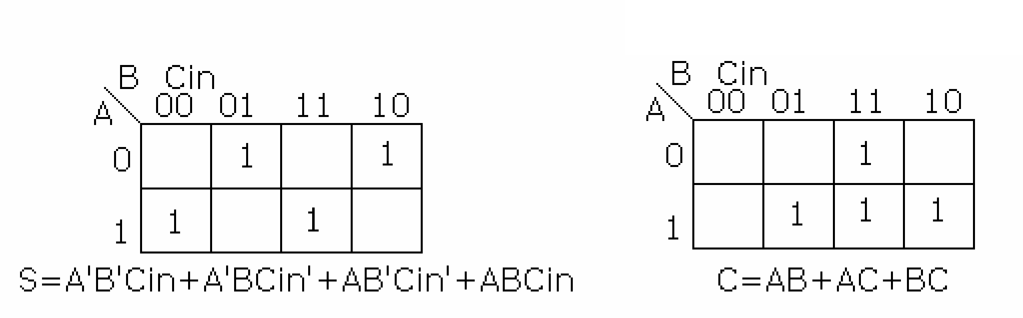
Figure 5 Full Adder Input/Output Components

The Full Adder Logic Circuit

At this point the technique for determining the actual logic circuit should be very obvious. Using the same technique as was used to design the *Half Adder*, we can now proceed with the design. The truth-table representing the system can be reconstructed with the appropriate logic expressions added to the lines whose outputs are "1".

Binary Inputs to be Summed				**Output "Sum" Result**			**Output "Carry" Result**	
C_{n-1}	***A_n***	***B_n***		***S_n***	***S_n (Expression)***		***C_n***	***C_n (Expression)***
0	0	0		0	.		0	.
0	0	1		1	$\overline{C}_{n-1}\ \overline{A}_n\ B_n$		0	.
0	1	0		1	$\overline{C}_{n-1}\ A_n\ \overline{B}_n$		0	.
0	1	1		0	.		1	$\overline{C}_{n-1}\ A_n\ B_n$
1	0	0		1	$C_{n-1}\ \overline{A}_n\ \overline{B}_n$		0	.
1	0	1		0	.		1	$C_{n-1}\ \overline{A}_n B_n$
1	1	0		0	.		1	$C_{n-1}\ A_n\ \overline{B}_n$
1	1	1		1	$C_{n-1}\ A_n\ B_n$		1	$C_{n-1}\ A_n\ B_n$

A full-adder is a combinational circuit that forms the arithmatic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by A and B, represent the two significant bits to be added. The Third input Cin represents the carry from the previous lower significant position. Two outputs are necessary because the arithmetic sum of three binary digits ranges in value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols S for sum and C for carry. The binary variable S gives the value of the least significant bit of the sum. The binary variable C gives the output carry. The truth table of full-adder is



A \ B Cin	00	01	11	10
0		1		1
1	1		1	

S=A'B'Cin+A'BCin'+AB'Cin'+ABCin

A \ B Cin	00	01	11	10
0			1	
1		1	1	1

C=AB+AC+BC

Figure 6: Maps for a full-adder

A full-adder can be implemented with two half-adders and one OR gate.

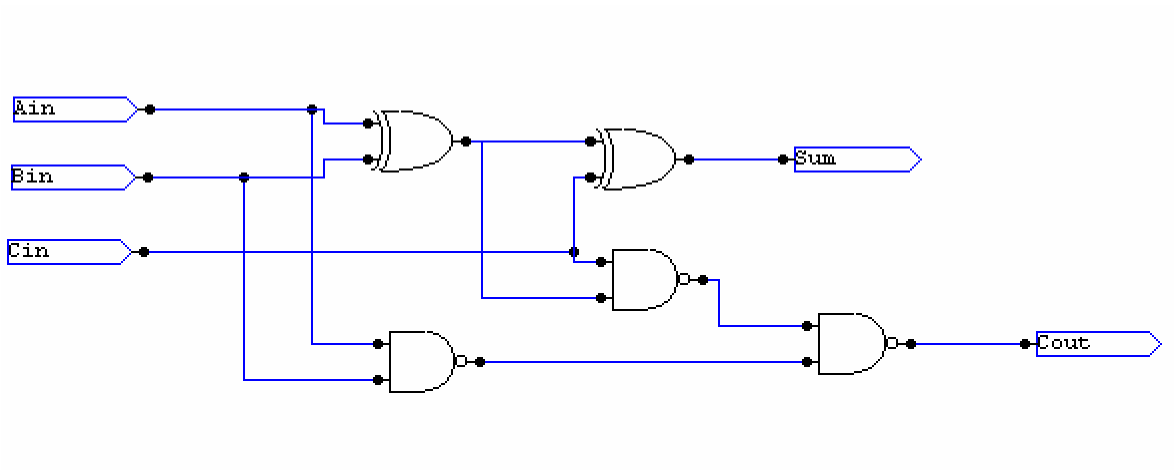


Figure 7: Implementation of a full-adder with two Half-adders and an OR gate

NAND Gate

The circuit diagram, the logic symbol, truth table and the layout diagram are given in the corresponding figures:

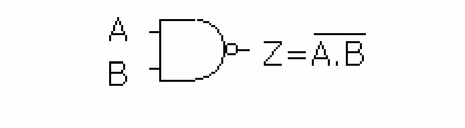


Figure 8 : Logic Symbol

Va	Vb	Vout
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

Figure 9: Truth Table

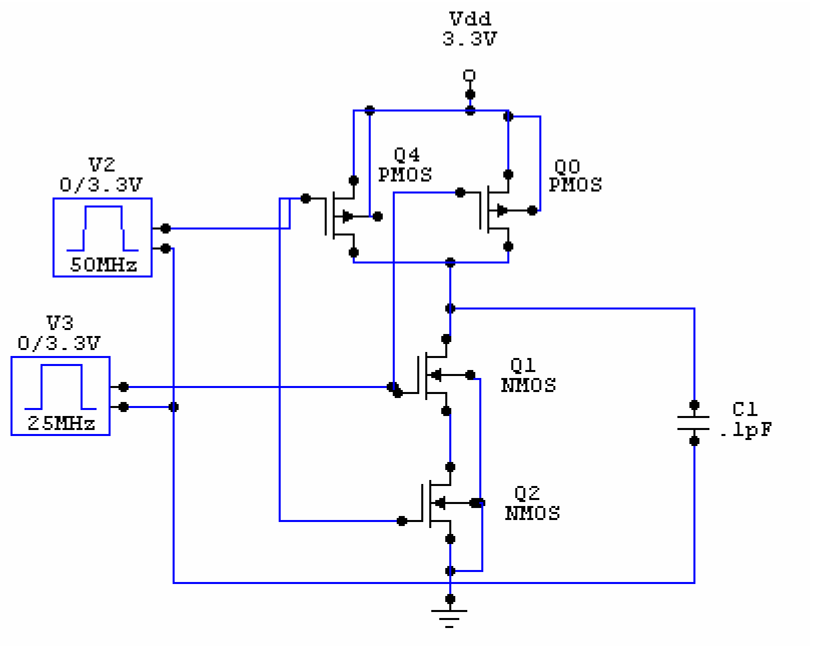


Figure 10: Circuit Diagram

A CMOS NOR2 gate and its complementary operation: Either the nMOS network is on and the pMOS network is off, or the pMOS network is on and the nMOS network is off.

Spice net-list for Circuit NAND

```
*Spice netlist for Circuit: nand.ckt

V1 6 0 DC 3.3V
V3 3 0 DC 0 PULSE(0 3.3 0 .1n .1n 20n 40n)
V2 5 0 DC 0 PULSE(0 3.3 0 .1n .1n 10n 20n)

MQ1 4 3 7 0 MNMOS l=0.6u w=4.8u
MQ2 7 5 0 0 MNMOS l=0.6u w=4.8u
MQ0 4 3 6 6 MPMOS l=0.6u w=9.2u
MQ4 4 5 6 6 MPMOS l=0.6u w=9.2u
C1 4 0 .1pF

.MODEL MNMOS NMOS
+ LEVEL=3 LD=0.1134U TOX=225.0E-10 XJ=0.2U
+ NSUB=1.968E+16 VTO=0.8186 KP=9.154E-05 GAMMA=0.5266
+ PHI=0.6 UO=596.5
+ DELTA=1.757 VMAX=1.942E+05
+ NFS=5.5E+12
+ RSH=116.5 TPG=1
+ CGDO=2.6106E-10 CGSO=2.6106E-10 CGBO=6.3402E-10 PB=0.8
+ CJ=3.1146E-04 MJ=.5 CJSW=4.3777E-10 MJSW=0.15423
.MODEL MPMOS PMOS
+ LEVEL=3 LD=0.1172U TOX=225.0E-10 XJ=0.2U
+ NSUB=1.514E+16 VTO=-0.9456 KP=3.1646E-05 GAMMA=0.4619
+ PHI=0.6 UO=206.2
+ DELTA=1.552 VMAX=4.441E+05
+ NFS=4.999E+12
+ RSH=129.5 TPG=-1
+ CGDO=2.6981E-10 CGSO=2.6981E-10 CGBO=8.6508E-10 PB=0.85
+ CJ=4.7864E-04 MJ=0.4973 CJSW=1.4771E-10 MJSW=0.190593
*#run
.tran .3n 60ns
*#plot v(3) v(5)
*#plot v(4)
.end
```

When either one or both inputs are high, i.e., when the n-net creates a conducting path between the output node and the ground, the p-net is cut-off. On the other hand, if both input voltages are low, i.e., the n-net is cut-off, then the p-net creates a conducting path between the output node and the supply voltage Vdd. Thus, the dual or complementary circuit structure allows that, for any given input combination, the output is connected either to Vdd or to ground via a low-resistance path. A DC current path between the Vdd and ground is not established for any of the input combinations. This yields the low-power operation mode for the simple CMOS inverter circuit.

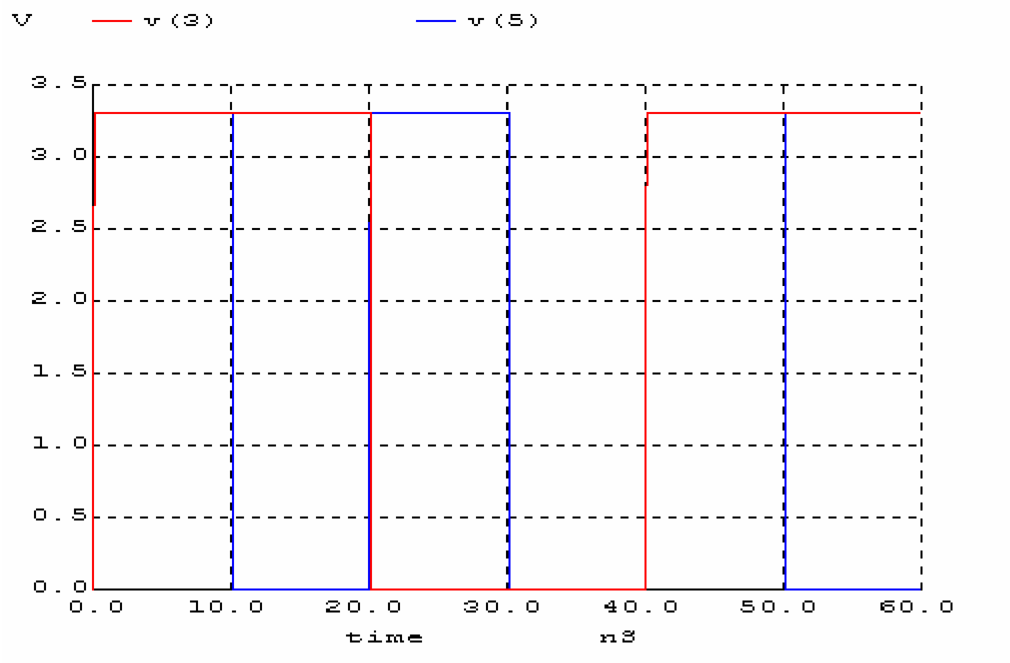


Figure 11: Timing Diagram, Input signals A and B

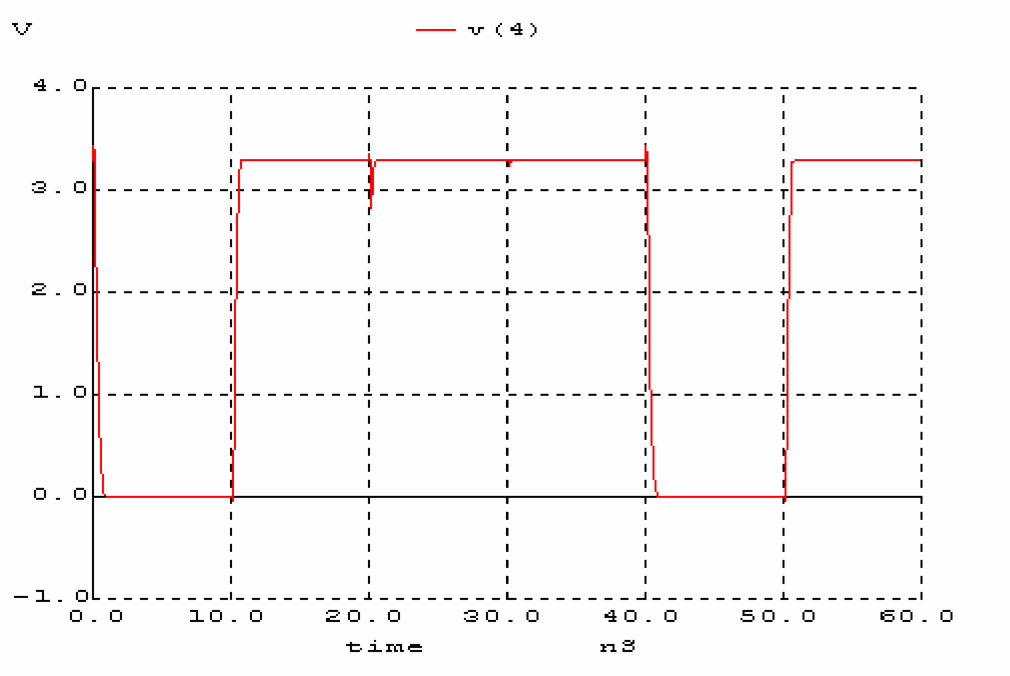


Figure 12: Timing Diagram, Output Signal for NAND Circuit

Delay in NAND Gate

The figure depicted below shows the delay for the NAND2 circuit in Figure 10. Figure 13 Shows the delay for 1pF load for NAND2 circuit.

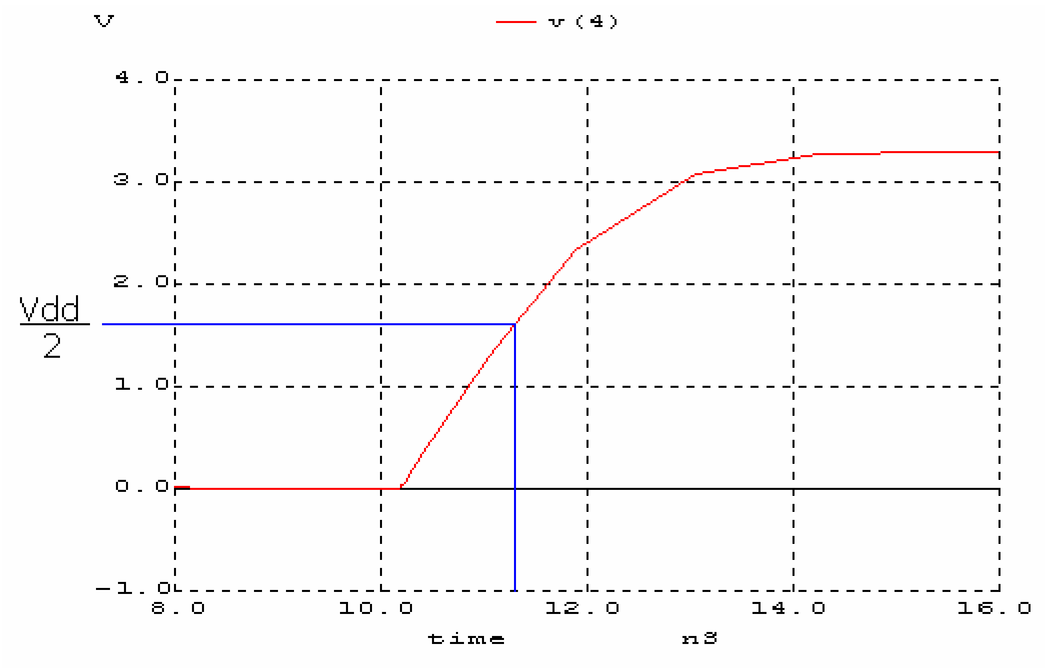


Figure 13: Delay in NAND Circuit for 1pF load.

We see that the delay is approximately less than 1 nS in order to reach a level of Vdd/2. The input signal comes at 10th second.

Figure 14 shows a sample layout of a CMOS NAND2 gate, using single-layer metal and single-layer polysilicon.p-well represented in yellow and n-well represented in green.

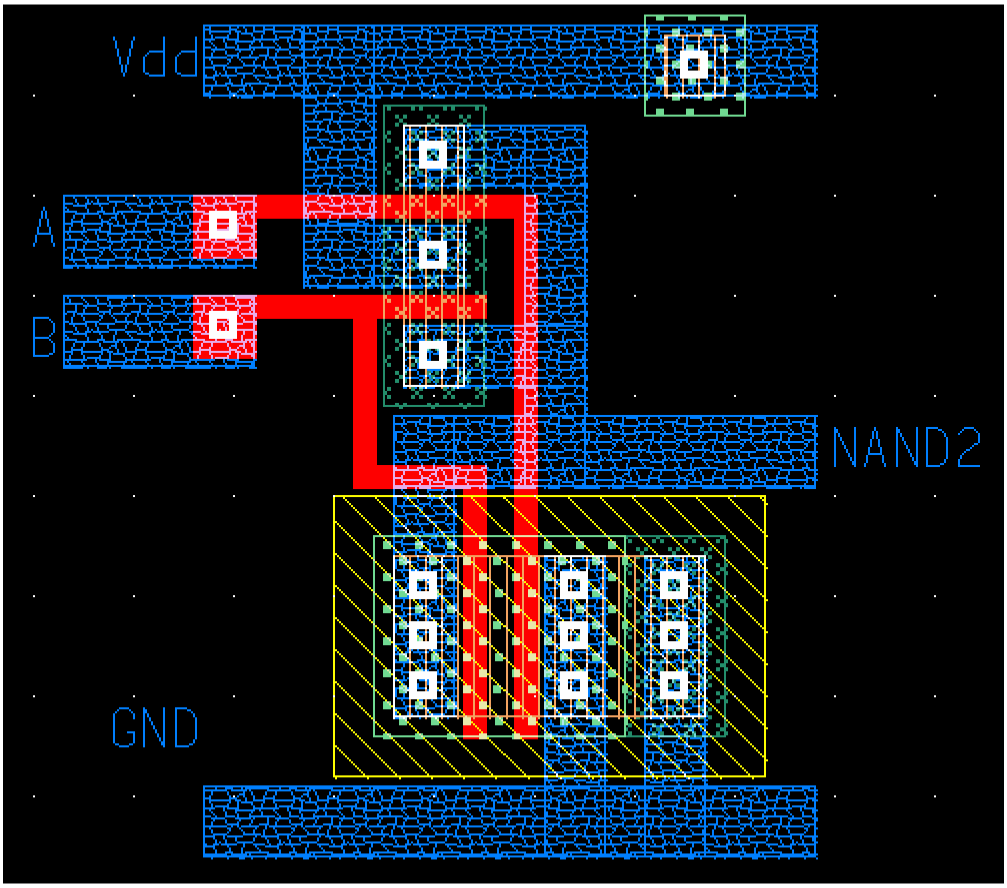


Figure 14: Layout Diagram of NAND Gate

ExOR Gate

The circuit diagram, the logic symbol, truth table and the layout diagram are given in the corresponding figures:

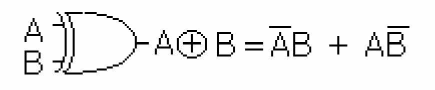


Figure 15: Logic Symbol

Vb	Vb	Vout
Low	Low	Low
Low	High	High
High	Low	High
High	High	Low

Figure 15: Truth Table of ExOR Gate

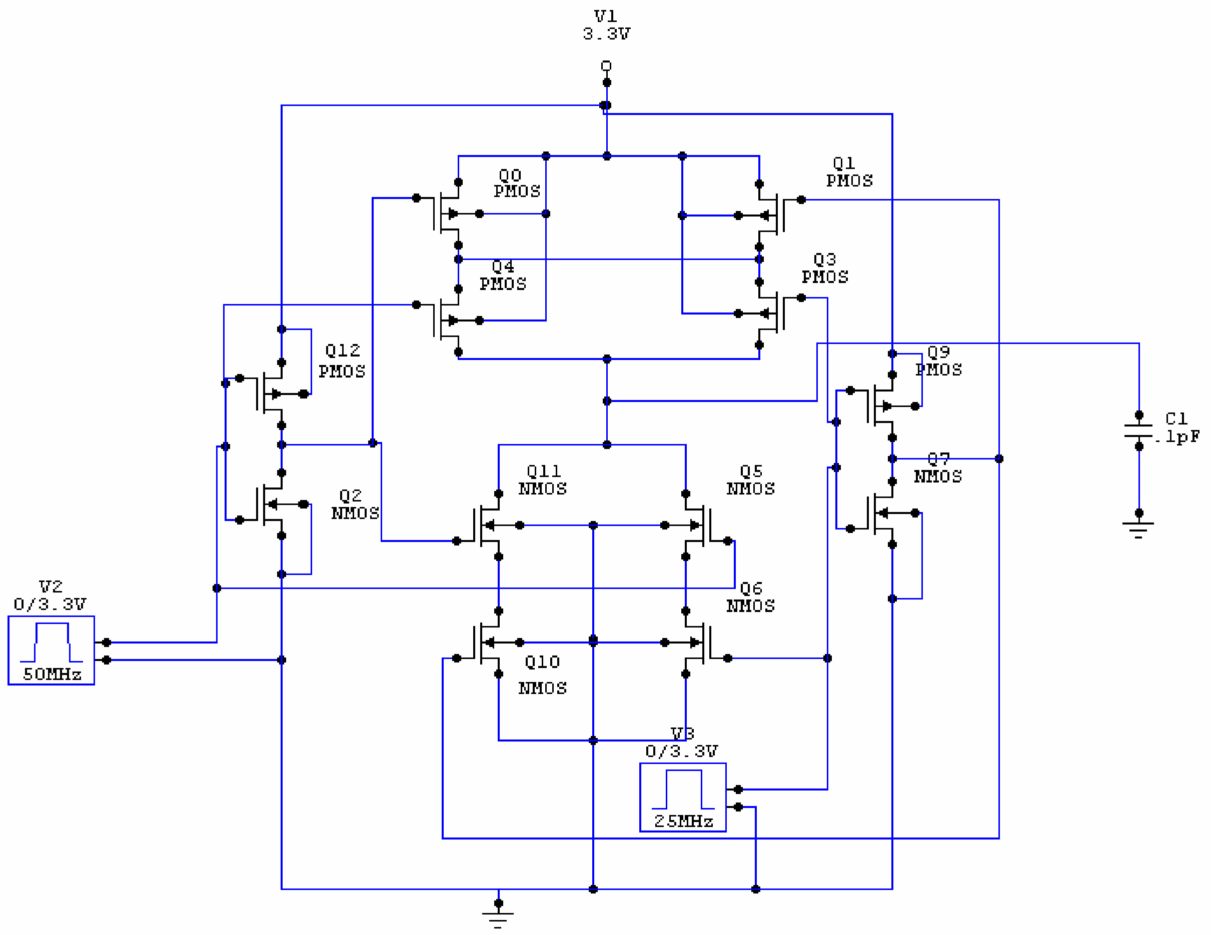


Figure 16: Circuit Diagram of ExOR Gate

The full implementation of the exclusive-Or function is shown in Figue 16. Additional inverters are also included in order to simulate the circuit. CMOS Ex-OR circuit requires a total of 12 transistors.

Spice net-list for Circuit Ex-OR Gate

```
*Spice netlist for Circuit:  exor.ckt
V1 10 0 DC 3.3V
V3 3 0 DC 0 PULSE(0 3.3 0 1n 1n 20n 40n)
V2 5 0 DC 0 PULSE(0 3.3 0 1n 1n 10n 20n)

MQ6 9 3 0 0 MNMOS L=0.6u W=4.8u
MQ5 7 5 9 9 MNMOS L=0.6u W=4.8u
MQ12 6 5 10 10 MPMOS L=0.6u W=28.8u
MQ7 4 3 0 0 MNMOS L=0.6u W=4.8u
MQ11 7 6 8 8 MNMOS L=0.6u W=4.8u
MQ1 11 4 10 10 MPMOS L=0.6u W=28.8u
MQ3 7 3 11 11 MPMOS L=0.6u W=28.8u
MQ2 6 5 0 0 MNMOS L=0.6u W=4.8u
MQ10 8 4 0 0 MNMOS L=0.6u W=4.8u
MQ0 11 6 10 10 MPMOS L=0.6u W=28.8u
```

```
MQ4 7 5 11 11 MPMOS L=0.6u W=28.8u
MQ9 4 3 10 10 MPMOS L=0.6u W=28.8u
C1 0 7 .1pF

.MODEL MNMOS NMOS
+ LEVEL=3 LD=0.1134U TOX=225.0E-10 XJ=0.2U
+ NSUB=1.968E+16 VTO=0.8186 KP=9.154E-05 GAMMA=0.5266
+ PHI=0.6 UO=596.5
+ DELTA=1.757 VMAX=1.942E+05
+ NFS=5.5E+12
+ RSH=116.5 TPG=1
+ CGDO=2.6106E-10 CGSO=2.6106E-10 CGBO=6.3402E-10 PB=0.8
+ CJ=3.1146E-04 MJ=.5 CJSW=4.3777E-10 MJSW=0.15423
.MODEL MPMOS PMOS
+ LEVEL=3 LD=0.1172U TOX=225.0E-10 XJ=0.2U
+ NSUB=1.514E+16 VTO=-0.9456 KP=3.1646E-05 GAMMA=0.4619
+ PHI=0.6 UO=206.2
+ DELTA=1.552 VMAX=4.441E+05
+ NFS=4.999E+12
+ RSH=129.5 TPG=-1
+ CGDO=2.6981E-10 CGSO=2.6981E-10 CGBO=8.6508E-10 PB=0.85
+ CJ=4.7864E-04 MJ=0.4973 CJSW=1.4771E-10 MJSW=0.190593
*#run
.tran .3n 100ns
*#plot v(3) v(5)
*#plot v(7)
.end
```

A CMOS Ex-OR gate and its complementary operation: Either the nMOS network is on and the pMOS network is off, or the pMOS network is on and the nMOS network is off.

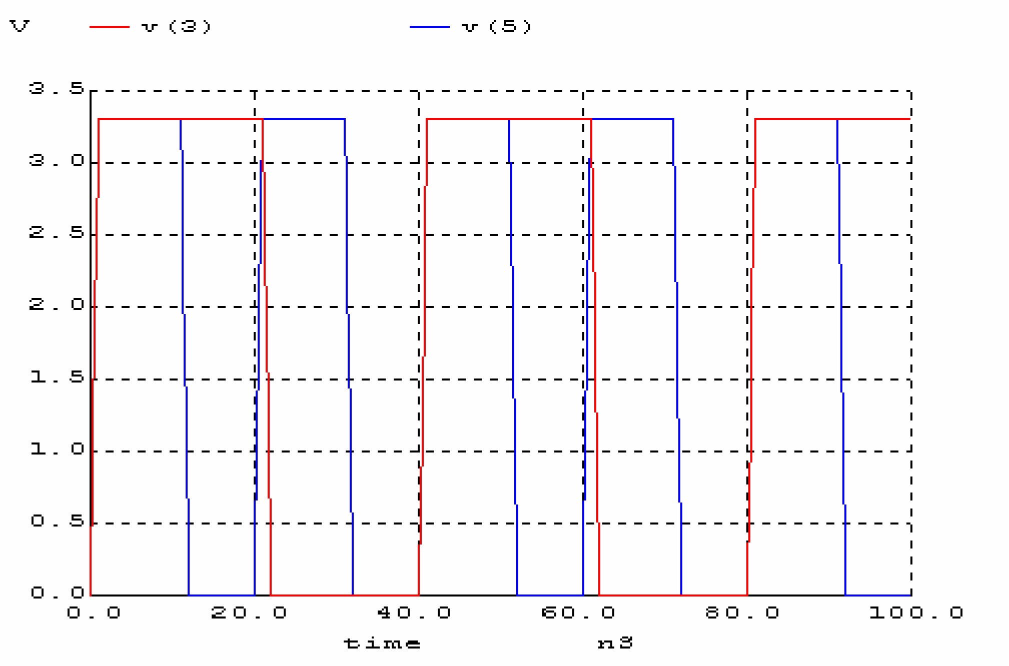


Figure 17: Timing Diagram, Input signals A and B

The input signals in the Figure 17 have 1nS rise times and 1nS fall times. So the output signal will be deformed from the edges

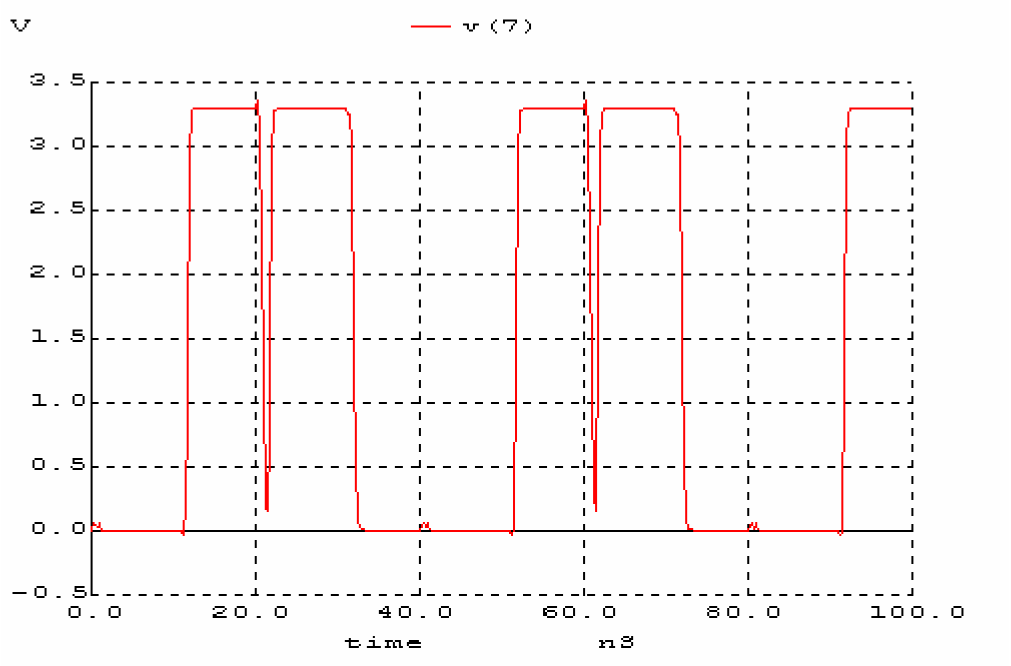


Figure 18: Timing Diagram, Output Signal for Ex-OR Circuit

Delay in Ex-Or Gate

The figure depicted below shows the delay for the Ex-OR2 circuit in Figure 16. Figure 19 Shows the delay for 1pF load for Ex-OR2 circuit.

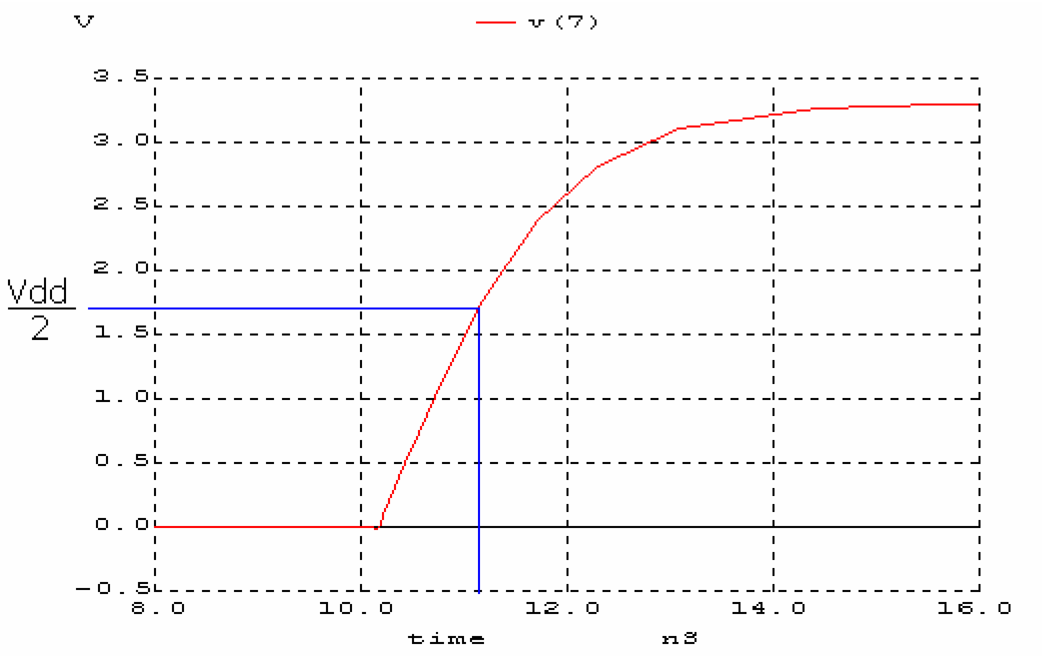
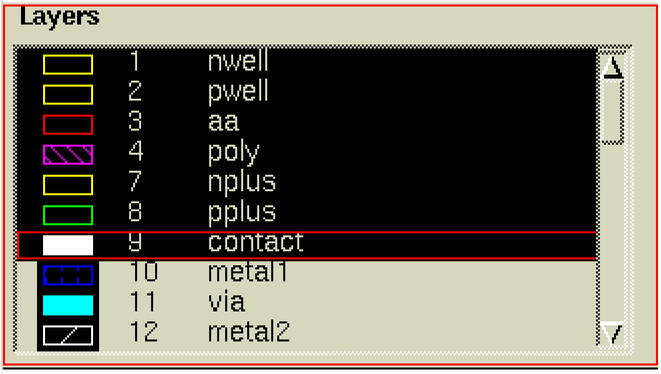


Figure 13: Delay in NAND Circuit for 1pF load.

In this circuit, we see that for 1pF load, the delay is less than 0.6 nS, the delay is few because the widths of the transistor is too big in order to handle more current.

Layout for Ex-OR Gate



Layers

□	1	nwell
□	2	pwell
□	3	aa
▨	4	poly
□	7	nplus
□	8	pplus
■	9	contact
▦	10	metal1
■	11	via
▧	12	metal2

Figure 19: Layers and contacts used in layouts

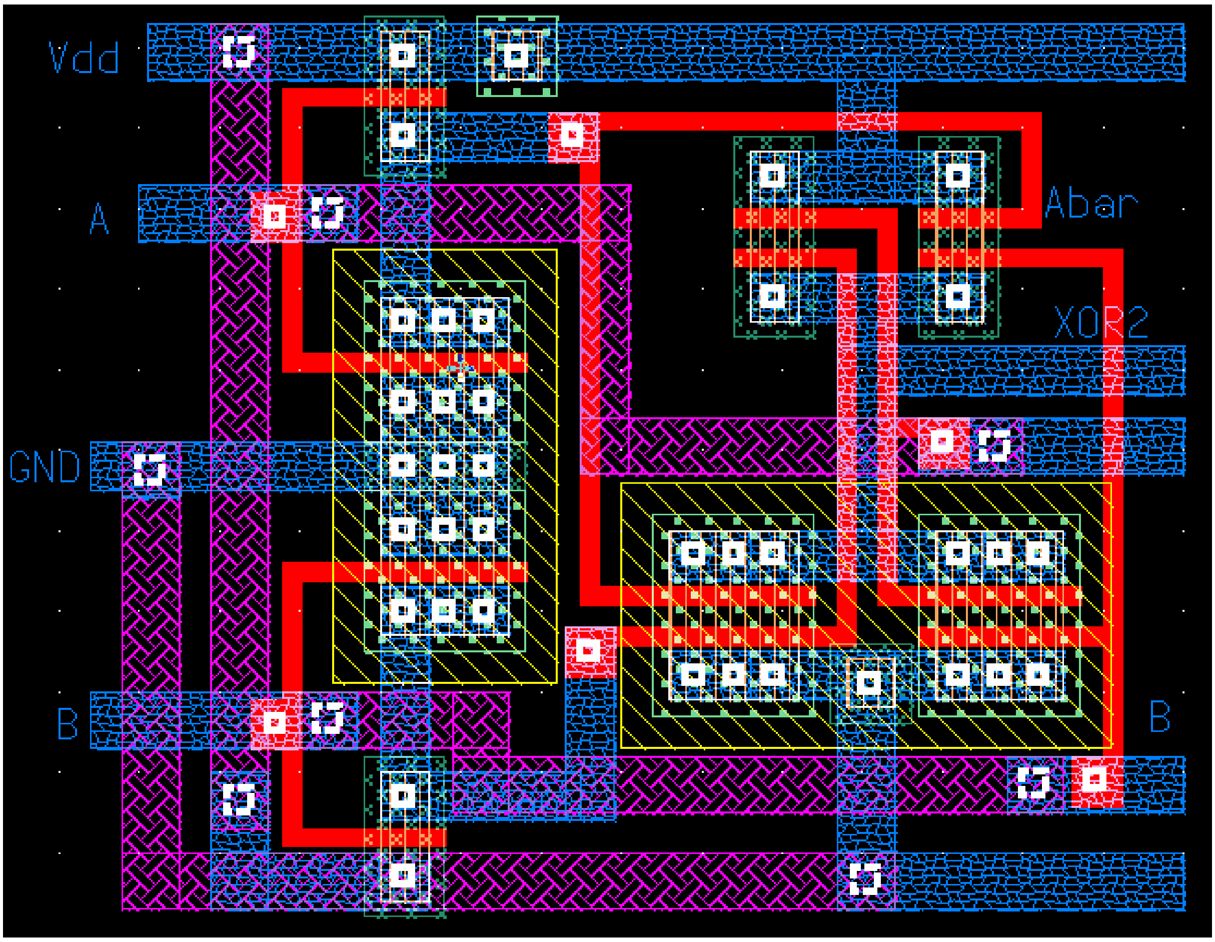


Figure 20: Layout Diagram of CMOS Ex-OR Gate

Full Adder Circuit

The full adder circuit is constructed from three NAND Gates and two Ex-OR Gates described above. The Full-Adder circuit consructed with NAND2 Gates and Ex-OR Gates took 36 transistors for one bit. The circuit diagram and the delays are shown in Figure 21.

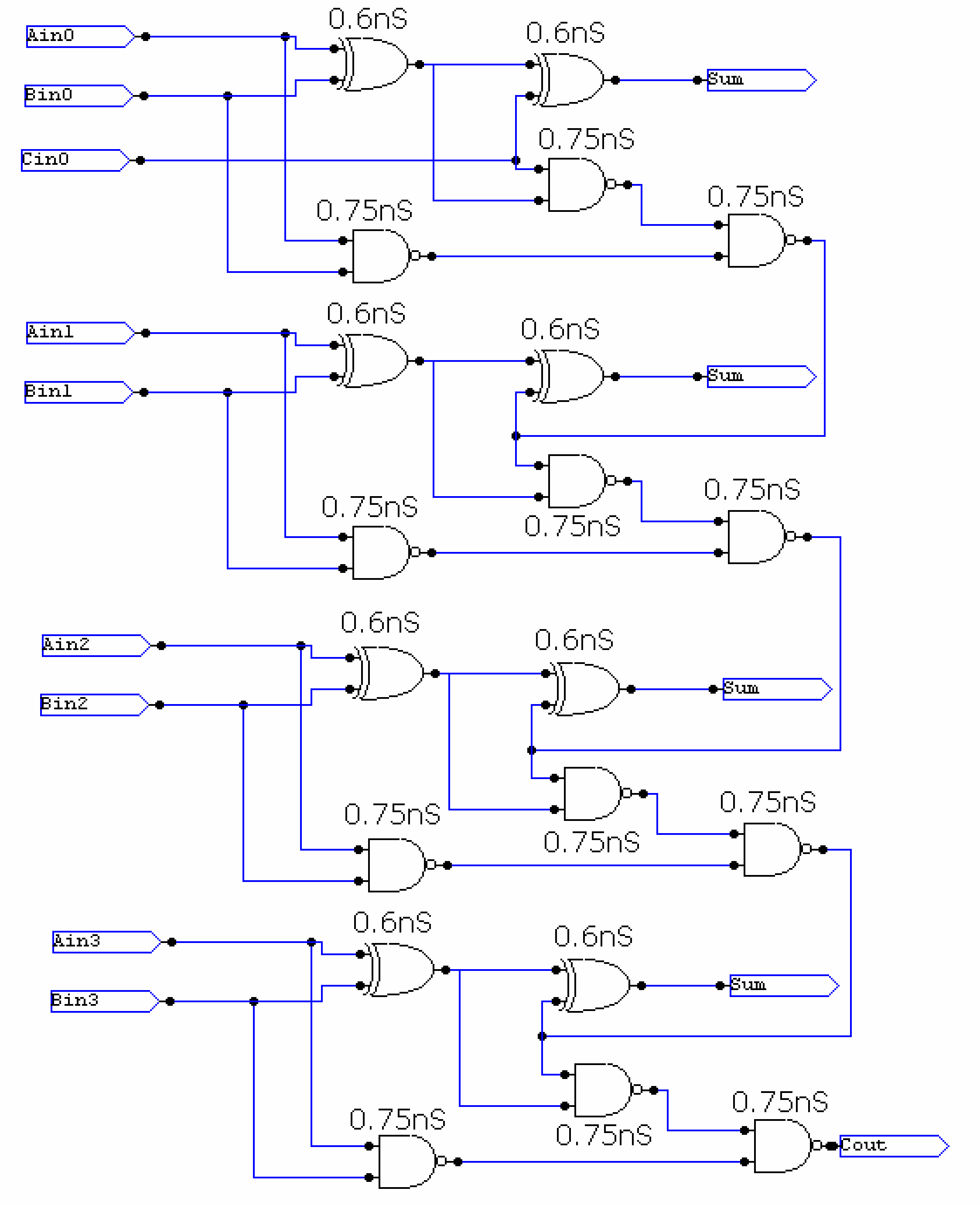


Figure 21: Circuit Diagram for 4 bit full adder

In order to find the total delay, we have to measure the output delay for the last carry. Here the critical path is the path going through NAND2 Gates. For 1 bit adder the total delay time is 2.25 nS and for 4 bit the total delay is 4*2.25nS = 9 nS.

Above the Spice net-list, simulation results delay graphs and the Layout diagram is depicted.

Spice net-list for Circuit Full-Adder

```
*Spice netlist for circuit 4 bit full adder

vdd VDD 0 3.3V
vgnd GND 0 0
vcin 9 0 0
Va1 10 0 DC 0 PULSE(0 3.3 0 .1n .1n 10n 20n)
Vb1 11 0 DC 0 PULSE(0 3.3 0 .1n .1n 20n 40n)
Va2 12 0 DC 0 PULSE(0 3.3 0 .1n .1n 40n 80n)
Vb2 13 0 DC 0 PULSE(0 3.3 0 .1n .1n 80n 160n)
Va3 14 0 DC 0 PULSE(0 3.3 2.5n .1n .1n 10n 20n)
Vb3 15 0 DC 0 PULSE(0 3.3 2.5n .1n .1n 20n 40n)
Va4 16 0 DC 0 PULSE(0 3.3 2.5n .1n .1n 40n 80n)
Vb4 17 0 DC 0 PULSE(0 3.3 2.5n .1n .1n 80n 160n)

x1 10 11 9 C1 S1 VDD GND adder
x2 12 13 C1 C2 S2 vdd GND adder
x3 14 15 C2 C3 S3 VDD GND adder
x4 16 17 C3 C4 S4 VDD GND adder

.SUBCKT adder ain bin cin cout sum vddp gnd
* nodes : Ain Bin Cin Cout Sum Vdd
m0 4 bin vdd vdd p l=0.6u w=3.6u
m1 vdd ain 6 vdd p l=0.6u w=3.6u
m2 22 ain vdd vdd p l=0.6u w=3.6u
m3 23 6 vddp vdd p l=0.6u w=3.6u
m4 7 4 22 vdd p l=0.6u w=3.6u
m5 7 bin 23 vdd p l=0.6u w=3.6u
m6 8 ain vddp vdd p l=0.6u w=3.6u
m7 vdd bin 8 vdd p l=0.6u w=3.6u
m8 10 cin vdd vdd p l=0.6u w=3.6u
m9 vdd 7 11 vdd p l=0.6u w=3.6u
m10 24 7 vdd vdd p l=0.6u w=3.6u
m11 25 11 vdd vdd p l=0.6u w=3.6u
m12 sum 10 24 vdd p l=0.6u w=3.6u
m13 sum cin 25 vdd p l=0.6u w=3.6u
m14 13 7 vdd vdd p l=0.6u w=3.6u
m15 vdd cin0 13 vdd p l=0.6u w=3.6u
m16 cout 13 vdd vdd p l=0.6u w=3.6u
m17 vdd 8 cout vdd p l=0.6u w=3.6u
m18 gnd bin 4 gnd n l=0.6u w=9.6u
m19 6 ain gnd gnd n l=0.6u w=9.6u
m20 15 4 gnd gnd n l=0.6u w=9.6u
m21 7 6 15 gnd n l=0.6u w=9.6u
```

```
m22 16 bin gnd gnd n l=0.6u w=9.6u
m23 7 ain 16 gnd n l=0.6u w=9.6u
m24 17 bin gnd gnd n l=0.6u w=3.6u
m25 8 ain 17 gnd n l=0.6u w=3.6u
m26 gnd cin 10 gnd n l=0.6u w=9.6u
m27 11 7 gnd gnd n l=0.6u w=9.6u
m28 18 10 gnd gnd n l=0.6u w=9.6u
m29 sum 11 18 gnd n l=0.6u w=9.6u
m30 19 cin gnd gnd n l=0.6u w=9.6u
m31 sum 7 19 gnd n l=0.6u w=9.6u
m32 20 cin gnd gnd n l=0.6u w=3.6u
m33 13 7 20 gnd n l=0.6u w=3.6u
m34 21 8 gnd gnd n l=0.6u w=3.6u
m35 cout 13 21 gnd n l=0.6u w=3.6u
c1 cout  0.500pF
.ENDS adder



.MODEL n NMOS
+ LEVEL=3 LD=0.1134U TOX=225.0E-10 XJ=0.2U
+ NSUB=1.968E+16 VTO=0.8186 KP=9.154E-05 GAMMA=0.5266
+ PHI=0.6 UO=596.5
+ DELTA=1.757 VMAX=1.942E+05
+ NFS=5.5E+12
+ RSH=116.5 TPG=1
+ CGDO=2.6106E-10 CGSO=2.6106E-10 CGBO=6.3402E-10 PB=0.8
+ CJ=3.1146E-04 MJ=.5 CJSW=4.3777E-10 MJSW=0.15423
.MODEL p PMOS
+ LEVEL=3 LD=0.1172U TOX=225.0E-10 XJ=0.2U
+ NSUB=1.514E+16 VTO=-0.9456 KP=3.1646E-05 GAMMA=0.4619
+ PHI=0.6 UO=206.2
+ DELTA=1.552 VMAX=4.441E+05
+ NFS=4.999E+12
+ RSH=129.5 TPG=-1
+ CGDO=2.6981E-10 CGSO=2.6981E-10 CGBO=8.6508E-10 PB=0.85
+ CJ=4.7864E-04 MJ=0.4973 CJSW=1.4771E-10 MJSW=0.190593
*#run
.tran .3n 180ns
*#plot v(10) v(12)
*#plot v(C1) v(S1)
*#plot v(C2) v(S2)
*#plot v(C3) v(S3)
*#plot v(C4) v(S4)
.end
```

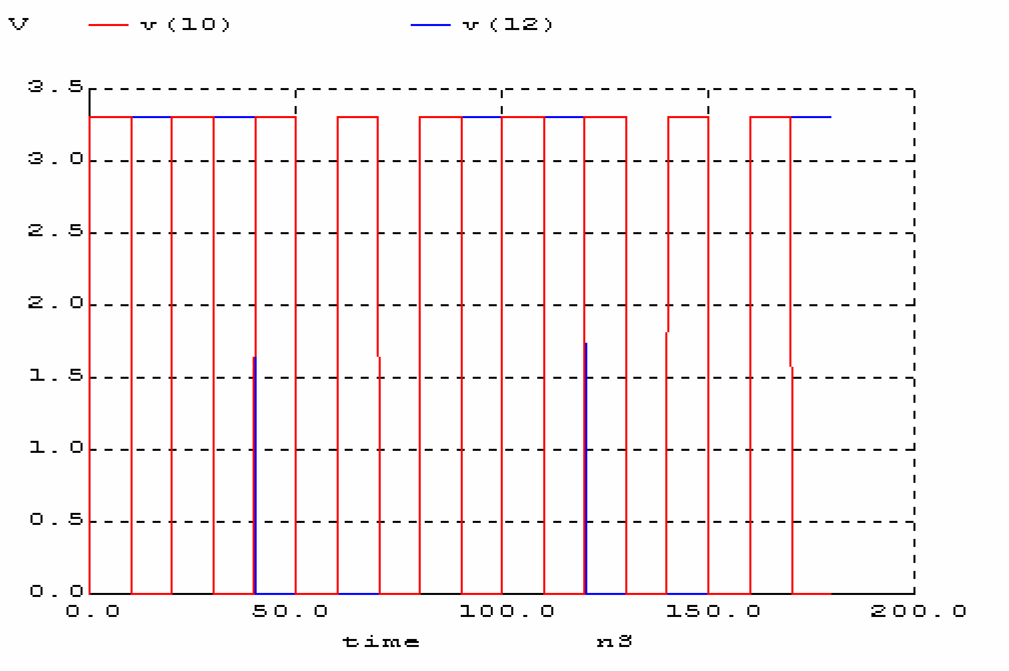


Figure 22: Timing Diagram, first two Input signals A and B

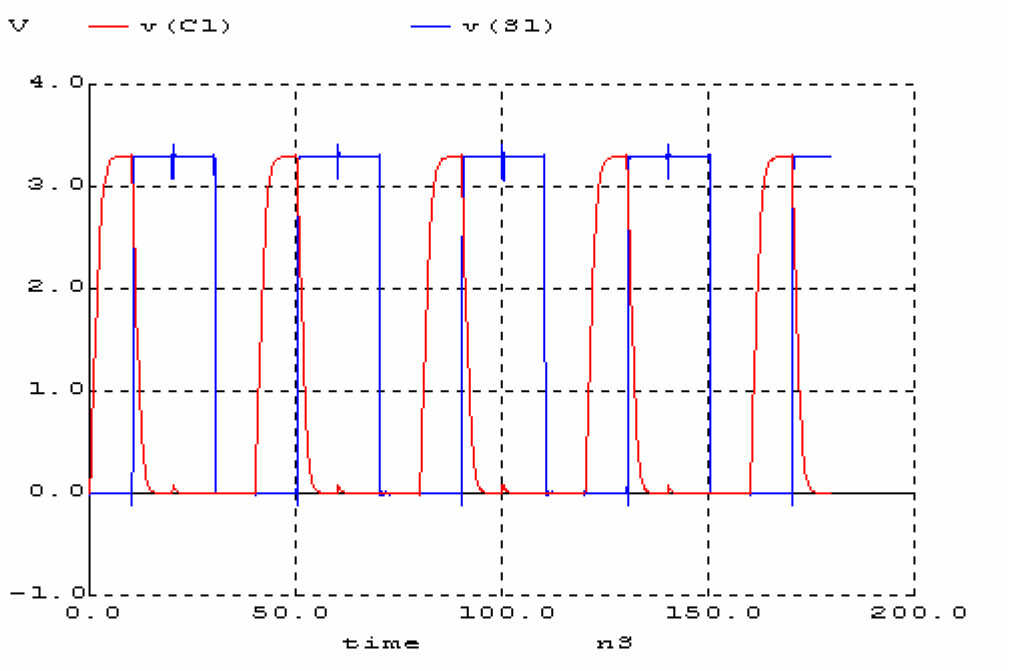


Figure 23: Timing Diagram, First Carry Output v(C1) and the Fist Sum output v(S1)

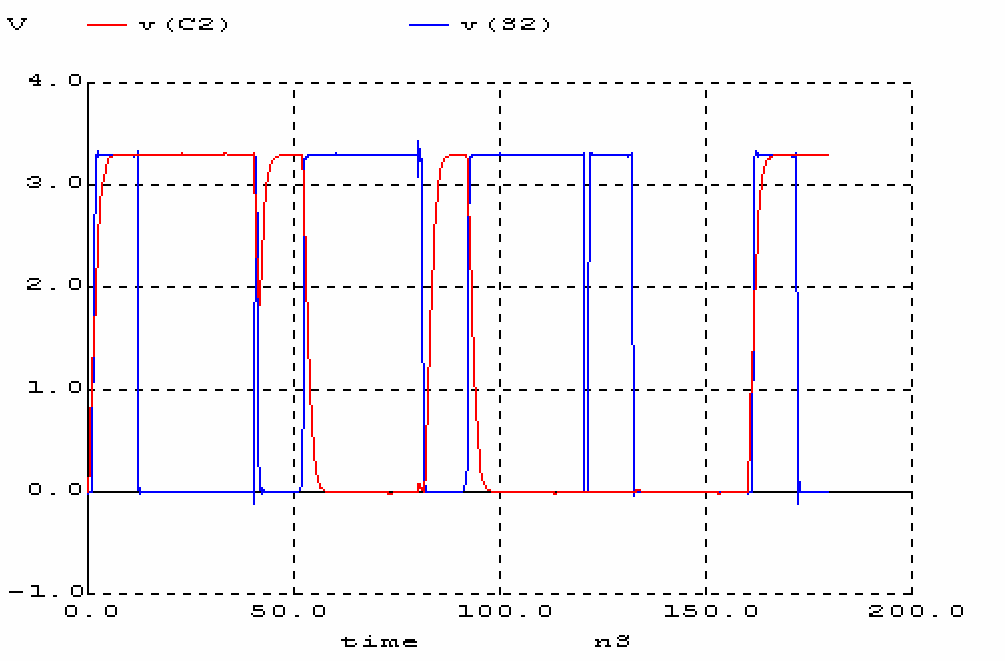


Figure 24: Timing Diagram, First Carry Output v(C2) and the Fist Sum output v(S2)

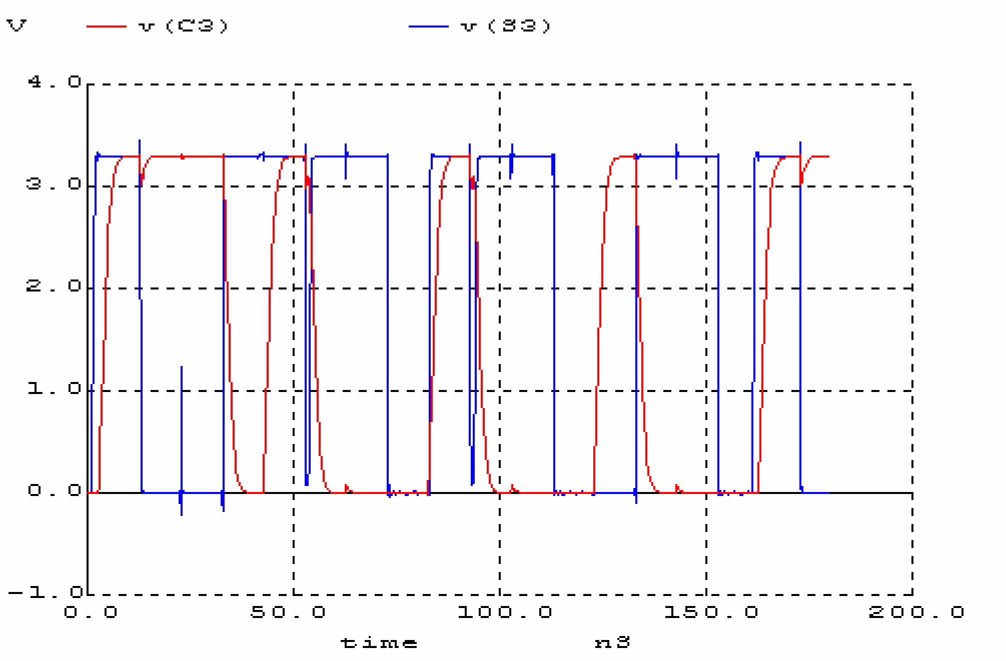


Figure 25: Timing Diagram, First Carry Output v(C3) and the Fist Sum output v(S3)

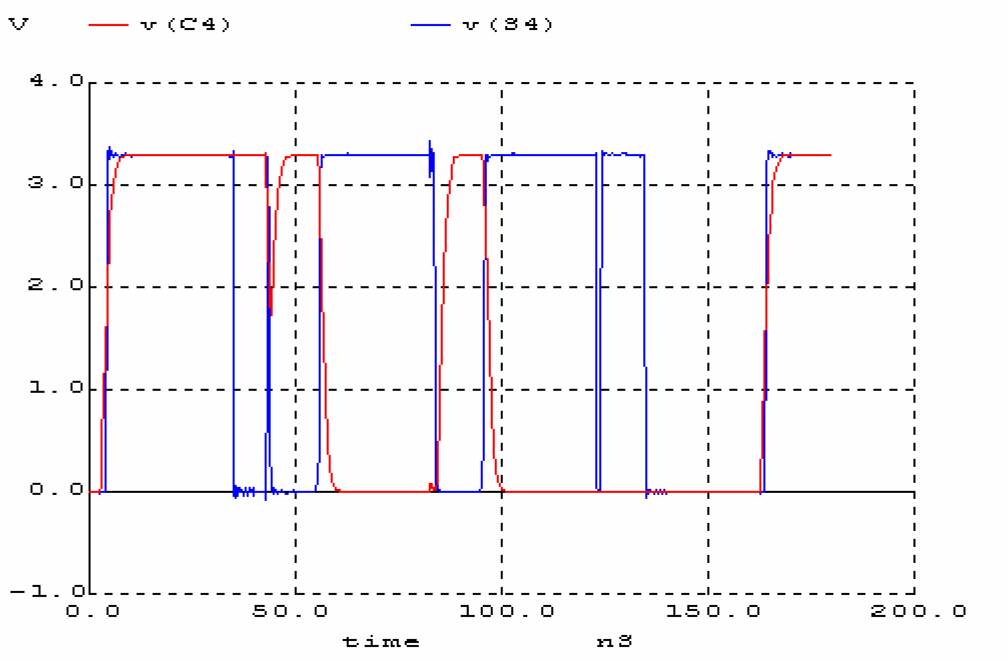


Figure 25: Timing Diagram, First Carry Output v(C3) and the Fist Sum output v(S3)

Delay in Full-Adder

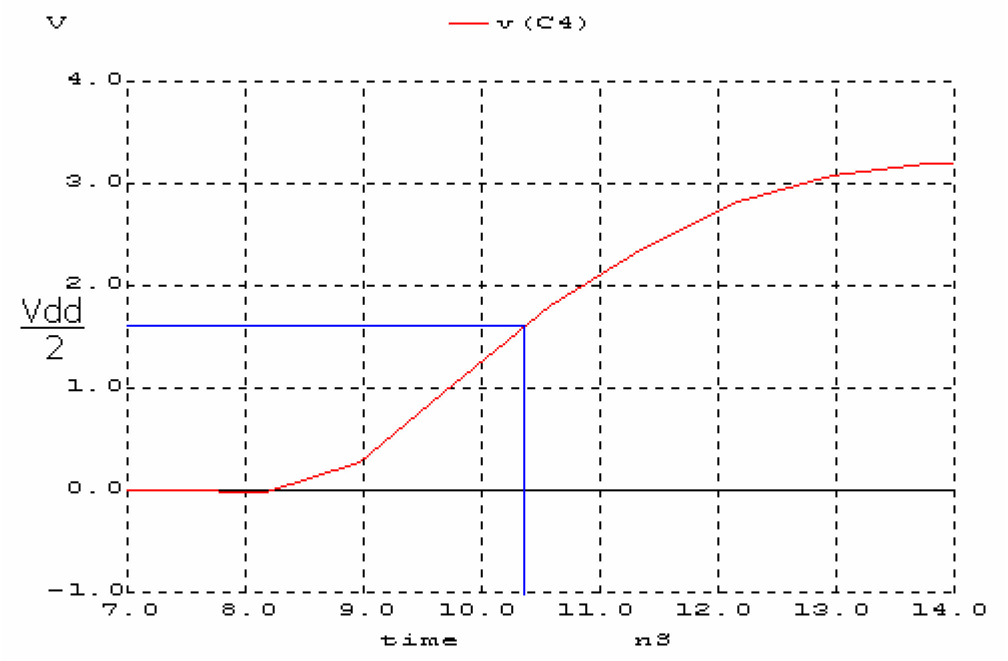


Figure 26: Delay in Full-Adder Circuit for 1pF load.

CRITICAL PATH

The critical path in our design is the very last Carryout bit. To determine delay, we just use the case of all the solution bits switching and see where does C4 stabilize (to within

10% of the final solution). And in Figure 26 we see that C4 reaches the final solution at about 10.5nS when the voltage (Vdd) is 3.3 Vdc.

Layout for 4-bit Adder

The simplest explanation of the layout is, the layouts for NAND2 Gate and Ex-OR gate depicted above, connected to form 1 Bit Adder.

The actual 4-bit adder circuit simply consists of four 1-bit adder modules.

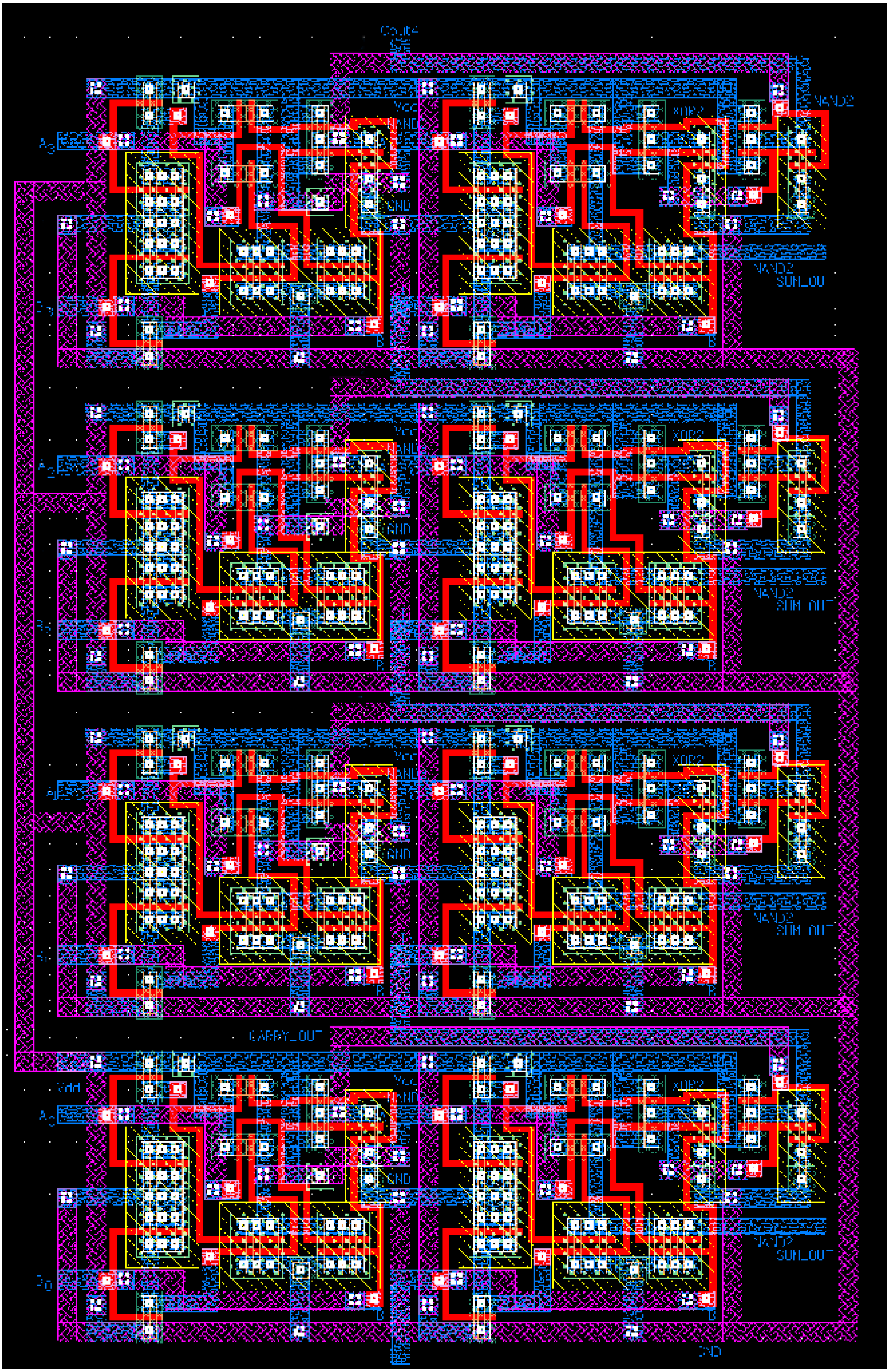

Cout4
Vcc
NAND
GND
XOR2
NAND2
A3
B3
NAND2
SUM_OUT
Vcc
NAND
GND
XOR2
A2
B2
NAND2
SUM_OUT
Vcc
NAND
GND
XOR2
A1
B1
NAND2
SUM_OUT
CARRY_OUT
Vdd
Vcc
NAND
GND
XOR2
A0
B0
NAND2
SUM_OUT
GND

Figure 27: Layout for 4-bit Full Adder Circuit.

Conclusion

Making designs with Spice is not sufficient for making a chip powerful, If we try to make the chip faster then we have to take into consideration that, the power consumption and the area of the chip will be larger. On the other hand we had limitations when doing this project, such that the maximum area that we have to choose was 2X and it sometimes takes time to configure the Mos-FET's to meet the requiretments like 2X limitation and 1pF loads. Ex-OR gate must be configured as 4X for P-MOS transistors and 2X for N-MOS transistors, because all connected in both series and parallel. And we expect some loss in the outputs of the circuit because of the 2X limitation.

At last, it is imposible to measure the power consumption with SPICE.

This was an interesting project. We taught the way integrated circuit chips can be designed and it gave the user (designer) the experience of seeing it can be tough designing integrated circuit chips but it also showed that there are many different ways to do your designs for your projects.

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